Amendments to the Specification:

Please replace paragraph [0023] with the following amended paragraph:

[0023] The first module may further send an address of a second module using the first set of signal lines, wherein the data bits are [[is]] sent by the first module to the second module in the data transfer phase (which follows the sending of the address). In one embodiment, the first set of signal lines comprise one of a request line on which a first module requests the message bus for transmission of data and a grant line on which the first module is indicated that the message bus has been granted.